REMARKS

Claims 1-2, 4-12, 14-22, 24-31 and 33-38 are rejected under 35 USC 103a as being unpatentable over Baird (USP 6,753,738) in view of Carroll (USP 5,130,571), prior art of record

Applicant asserts that Claims 1-2, 4-12, 14-22, 24-31 and 33-38 should not be found unpatentable over Baird (USP 6,753,738) in view of Carroll (USP 5,130,571) because there is no motivation for a person skilled in the art to combine the teachings of Baird with those of Carroll to result in the present invention as claimed in Claims 1-2, 4-12, 14-22, 24-31 and 33-38. In particular, both Carroll and Baird specifically teach against such a combination.

Baird, in numerous locations throughout his description, teaches a slow change in the capacitance of the switched capacitors and therefore in the VCO frequency. For example:

In the abstract, "the second feedback loop is arranged to cause a slow enough change in the VCO frequency".

Col 3, lines 25-29, "the single bit which changes is preferable caused to achieve a controlled transition time (or ramp rate) which is slow enough to cause a very gradual change in the value of the associated tuning elements".

Col 3, lines 42-46, "The digital control signals are arranged to influence the feedback system slowly enough, relative to the first feedback loop, to allow the first feedback loop to adjust the control signal and maintain the controlled parameter substantially unchanged as the digital control signal changes value".

Col 5, lines 21-32, "Fig. 8 is a schematic diagram of a tank circuit including a variable capacitance circuit useful for gradual adjustment of the oscillation frequency of the tank circuit".

Col 10, lines 38-41, "group of variable capacitance circuit 299 whose gates are generally held staticly during operation, but which may be slowly switched on or off to gradually vary the amount of capacitance on nodes 146 and 148".

Col 11, lines 9-16, "Moreover, the slow digital control circuit 306 is preferably configured to provide a very slow rise time and fall time on whichever slow digital control signal VSD<i> changes logic state at any given time, while holding all other slow digital control signals quiescent at one of the static levels. This allows the value of the total capacitance to change much more slowly and reduces perturbations to the overall system."

Col 11, lines 17-20, "Referring now to Fig. 9, a gate control circuit 220 is shown which is an exemplary embodiment of the slow digital control circuit 306 and which accomplishes slow rise and fall times on its various gate control output signals."

Col 11, lines 29-33, "To achieve even slower transition times of the slow digital control signals, additional load capacitance, such as load capacitor 230, may be included on the various control signal output nodes, such as node 305N".

Col 11, lines 49-50, "a signal having a slow risetime and a slow falltime which is shared as needed to generate each switch control signal".

In contrast, Carroll teaches a switched capacitor circuit that uses more than one switch in parallel in order to allow a high-speed capacitor charge while reducing induced offset voltage. In particular:

In the abstract, "with a capacitor charge or acquisition time due to the parallel combinations of all of the switches".... "thus, a fast capacitor charge or acquisition time".

Col 1, lines 56-61, "The control signals of each switch are turned off in sequence giving an induced offset voltage in the final case due only to the last turned off switch, but with a capacitor charge or acquisition time due to the parallel

combinations of all of the switches".

Col 2, lines 13-17, "This results in a fast acquisition time followed by a reduction in voltage to the normal 'digital' level until turn off where the resultant induced offset voltage is the same as that due to a simple minimum sized switch".

Col 3, lines 16-18, "Therefore, the circuit 20 provides a fast acquisition due to transistor T24 and capacitor Cs, but the low offset voltage of the T22/Cs combination".

Applicant asserts that, as a whole, the teachings of Baird are directed at slowly changing the capacitance value of switched capacitors, while the teachings of Carroll, as a whole, are directed at a fast capacitor charge / acquisition time due to the parallel combination of switches in a switched capacitor circuit. Applicant therefore asserts that a person skilled in the art would not have any motivation to combine said references by replacing the single switch transistor shown in Baird with a plurality of differently sized switch transistors sequentially switched off with a smallest switch transistor being switched off last for the purpose of increasing speed with a minimal offset voltage to thereby result in the present invention, as was stated by the Examiner. The reason is that Baird teaches slow rising and falling control signals of the switches in order to deliberately result in slow transitions of the capacitance and therefore slow transitions of the VCO speed. The combination purpose of increasing the speed as stated by the Examiner directly conflicts with the very specific and clearly stated purpose of Baird.

For at least the above reason, applicant asserts that there is no motivation for a person skilled in the art to combine the teachings of Baird with those of Carroll to result in the present invention because there is no desirability of such a combination taught by Baird or Carroll. Reconsideration of Claims 1-2, 4-12, 14-22, 24-31 and 33-38 is respectfully requested.

Sincerely yours,

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